Case 7:25-cv-00183-ADA Document 29-13 Filed 10/31/25 Page 1 of 5

EXHIBIT 13

Case 7:25-cv-00283-ADA Document 29-12 Filed 00/04/25 Page 2 of 5

EXHIBIT 4

REDSTONE LOGICS, LLC

V_

NXP USA, INC.

Case No. 7:24-cv-00028-DC-DTG

REDSTONE LOGICS, LLC

V.

MEDIATEK, INC. and MEDIATEK USA, INC.

Case No. 7:24-cv-00029-DC-DTG

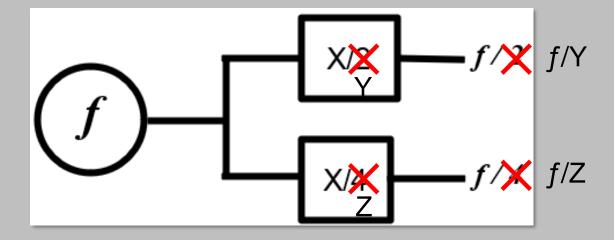
Redstone's *Markman* Presentation

February 19, 2025

"the first clock signal is independent from the second clock signal"

Redstones's Proposal	Preliminary Construction	NXP's Proposal
Plain and ordinary meaning	Plain and Ordinary Meaning	Plain and Ordinary meaning where the plain and ordinary meaning requires that the first and second clock signals are provided by or processed (i.e., divided or multiplied) from different reference oscillator clocks.

NXP's "Plain and Ordinary Meaning" is Wrong



Dkt. 43 at 2